

IN THE CLAIMS:

1. (Currently amended) A circuit comprising:
 - a plurality of data input terminals each for receiving respective serial data signals having the same bit rate,
 - bit clock generating means responsive to the serial data signals to provide for each a respective bit clock signal, and
 - a plurality of word forming means each connected to receive the bits of a respective one of the serial data signals for forming those bits into words and outputting the bits of those word in parallel,wherein the circuit further comprises a common word clock generating means for providing a common word clock in response to ~~[[the]]~~ phases of the ~~[[said]]~~ bit clock signals, and
 - each of the plurality of word forming means is so responsive to the common word clock signal to provide ~~[[its]]~~ the words aligned to the common word clock.
2. (Original) A circuit as claimed in claim 1 wherein the word clock generating means comprises a representative phase calculator for providing a phase signal representative of the phases of the plurality of bit clock signals, the word clock generating means being arranged to generate the common word clock so as to have the phase indicated by the representative phase signal or a phase derived therefrom.
3. (Original) A circuit as claimed in claim 2 wherein the word clock generating means is arranged to add, or subtract, an offset to the representative phase signal and to generate the common word clock so as to have the phase indicated by the result of that addition or subtraction.
4. (Original) A circuit as claimed in claim 1 wherein each word forming means comprises a shift register connected to receive serially the bits of the respective data signal and to shift them along the shift register in response to the respective bit clock signal.

5. (Original) A circuit as claimed in claim 4 wherein each said shift register comprises two component shift registers connected to receive the bits of the data signal alternately.

6. (Currently amended) A circuit as claimed in claim 3 wherein the word forming means comprises a register connected to latch bits from the shift register in parallel in response to the common word clock signal.

7. (Currently amended) A method receiving a plurality of serial data signals having the same bit rate comprising:

generating in responsive to the serial data signals a respective bit clock signal for each, and

forming bits of each serial data signal into parallel words,

wherein the method comprises providing a common word clock in response to ~~[[the]]~~ phases of the ~~[[said]]~~ bit clock signals, and the forming of the bits into words provides ~~[[those]]~~ the words aligned to the common word clock.

8. (Original) A method as claimed in claim 7 wherein the method comprises calculating a phase signal representative of the phases of the plurality of bit clock signals, generating the common word clock so as to have the phase indicated by the representative phase signal or a phase derived therefrom.

9. (Original) A method as claimed in claim 8 wherein the method comprises adding, or subtracting, an offset to the representative phase signal and generating the common word clock so as to have the phase indicated by the result of that addition or subtraction.